REMARKS

Examiner Steven Loke is thanked for his examination of the subject Patent Application. The Specification and Claims have been carefully reviewed, the Claims amended and all Claims are considered to be in condition for Allowance.

Claim Status

Claims 29, 33-35 remain in this application. Claims 29 and 33 have been amended.

Action Item 1

Abstract Correction

> 1. The abstract of the disclosure is objected to because the abstract should disclose the structure of the device instead of the method to make the device. The claimed invention is directed to a device structure, Correction is required.

The abstract has been amended to read on a structure.

Action Items 2 & 3

35 U.S.C.112, first paragraph

2. Reconsideration of the rejection of Claim 33 under 35 U.S.C.112, first paragraph, as failing to comply with the written description requirement is requested based on the following reasons.

The Examiner writes:

> Original claim33 discloses the opening has a width between about 1500 to 5000 angstroms, The specification never discloses the opening has a width between about 1500 to 35000 angstroms as claimed in claim 33.

Claim 33 has been amended to correct a typographical. It is 5000, not 35000 angstroms.

> 3. Claim 29 is objected to because of the following informalities: line 21, the phrase "a self-aligned source.(SAS) line" is unclear ... Appropriate correction is required.

Claim 29 has been amended by removing the redundant abbreviations.

Action Item 4

35 U.S.C.112, second paragraph

4. Reconsideration of the rejection of Claims 29 and 33-35 under 35 U.S.C.112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter" which applicant regards as the invention is requested based on the following reasons.

The Examiner writes:

> Claim 29, lines 4-5, the phrase "at least two trenches formed to a depth between "about 2500 to 5000 angstroms below the surface of said substrate" is unclear whether it is being referred to "at least two trenches each formed to a depth between about 2500 to 5000 angstroms below the surface of said substrate"; lines 6-7, the phrase "an oxide layer formed over said substrate, including over the inside walls of said two trenches" is unclear whether it is being referred to "an oxide layer formed over said substrate, including over the inside walls of each of said two trenches".
>
> Claim 29, line 8, the phrase "a high-step oxide formed within said two trenches over the oxide layer..." is unclear. Fig. 8 discloses a high-step oxide [250] formed within each of the two trenches over the corresponding oxide layer [240]. It is believed that a high-step oxide formed within each of said two trenches over the corresponding oxide layer in claim 29.
>
> Claim 29, lines 11-12, the phrase "said high-step oxide forming an opening with high walls over the surface of said substrate between said two trenches" is unclear whether it is being referred to "two of said high-step oxides forming an opening with high walls over the surface of said substrate between said two trenches".

Response: Claim 29 has been amended to clarify these descriptions of the structure.

Action Items 5 & 6

35 USC 112

6. Reconsideration of the rejection of Claims 29, 34 and 35 insofar, as in compliance with 35 USC 112, under 35 U.S.C. 103(a) as being unpatentable over

Acocella et al. is requested based on the following arguments.

The Examiner writes:

> In regards to claim 29, Acocella et al. disclose a stacked-gate flash memory having a shallow trench isolation with a **high-step oxide** [12] in fig. 1. It comprising: a substrate [11] having a gate oxide layer [13]; at least two trenches (the two trenches that formed under the oxide layers [12]) each having a depth; an oxide layer (a bottom portion of the oxide layer [12] that formed along the bottom and sidewalls of the trench) formed over the substrate, including over the inside walls of each of the two trenches; a **high-step oxide** (a top portion of the oxide layer [12]) formed within each of the two trenches over the oxide layer (a bottom portion of the oxide layer [12] that formed along the bottom and sidewalls of the trench) and protruding upward over the surface of the substrate to a height; two of the high-step oxides forming an opening with high walls over the surface of the substrate between the two trenches; a first conductive layer [14] formed conformally inside and extending above the opening and **over the surface of the substrate** between the high walls to form a floating gate having internal and external folding surfaces; an intergate oxide layer [15] formed over the internal and external folding surfaces of the floating gate [14]; a second conductive layer [16] formed protruding downward in between said internal and external folding surfaces over the intergate oxide layer [15] to form a control gate [16]. Since the floating gate [16] has folding surfaces, it is inherent that there is high lateral coupling between the floating gate and the control gate.

The Applicants reply by saying that Fig. 1, a prior art, of Acocella et al. resembles instant Fig. 3e in several ways except for several major differences.

Firstly, Acocella et al. say that Fig. 1 is a highly simplified diagram that **they do not admit to being prior art**. In other words Fig. 1 is not therein disclosed as representing any prior art nor their invention and therefore it is fiction. It is used together with the highly simplified Fig. 2 to illustrate their invention, that of eliminating undulating surfaces as shown in Fig. 1 in favor of the smooth surfaces of Fig. 2 in order to eliminate defects in the intergate dielectric layer when thin dielectric layers are employed to increase the capacitance coupling. In other words, Fig. 1 as a fiction is used to teach away from the teaching of the instant invention.

Acocella et al. Column 4 line 3:

> Referring now to the drawings, and more particularly to FIG. 1, there is shown, in

highly simplified form, an EEPROM gate structure 10 over which the present invention is an improvement. **It is to be understood in this regard that no portion of FIG. 1 is admitted to be prior art as to the present invention. Rather, this highly simplified diagram is provided in an effort to provide an improved understanding of the problems which are overcome by the invention.** In this structure, recessed oxide (ROX) 12 is used for isolation between adjacent gates. As will be discussed below in regard to operation of a preferred form of a flash memory in accordance with the invention, it is preferred that transistors including a floating gate for storage of charge be formed in very close proximity since the memory cells are programmed through a series connection of the source and drain regions of a plurality of such transistors. Therefore, isolation is generally necessary to minimize interaction between memory cells formed by those transistors.

Secondly, Acocella et al. do not teach forming a **high-step oxide** for increased coupling purposes. They teach to make the oxide height sufficient to define the thickness of their floating gate.

Acocella et al. Column 5, line 48:

As shown in FIG. 5, certain areas of the substrate are recessed by etching, using a further mask (not shown) and recessed oxide isolation structures 38, 38' are formed which rise above the substrate surface. **The dimension of rise of the ROX isolation structures should be controlled by control of oxidation time since they eventually will define the thickness (e.g. about 2000 Angstroms) of the floating gate structure.** These isolation structures are located at the boundaries of the p-wells 32, 33 and n-well(s) 36 and at the locations where boundaries of other structures will be formed. The ROX isolation structures formed over p-well 33, where the memory cell array will be formed is actually a layer indicated by dashed line 37 having long, narrow rectangular apertures bounded at the ends by ROX structures 38'. These rectangular apertures are shown more clearly at 1501 of the plan view of the device as illustrated in FIG. 15. Within these rectangular apertures the nitride/oxide layer 34 may now be readily stripped away.

Therefore Acocella et al. does **not** teach high step oxides, oxide steps purposely made multifold higher than the thickness of the floating gate. And Acocella et al. does not illustrate prior art when they use Fig. 1.

The Examiner continues with:

Acocella et al. differ from the claimed invention by not showing the at least two trenches each formed to a depth between about 2500 to 5000 angstroms below the . surface of the substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the at least two trenches each formed to a depth between about 2500 to 5000 angstroms below the surface of the substrate, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable

ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Acocella et al. differ from the claimed invention by not showing the high-step oxide formed within each of the two trenches over the oxide layer and protruding upward over the surface of the substrate to a height between about 2000 to 6000 angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the high-step oxide formed within each of the two trenches over the oxide layer and protruding upward over the surface of the substrate to a height between about 2000 to 6000 angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

The Applicants reply that there is a major difference in point here. As said above, the instant objective is to make the "high step" oxide taller than the maximum thickness of the floating gate in order to get maximum folding or vertical coupling. The object of Acocella et al. is to make the "step" oxide essentially the same height as the thickness of the floating gate in order to form a flat floating gate. Therefore it is not an issue of discovering an optimum or workable range to cause citing In re Aller. It is an issue of which direction these two structures teach. The Applicants assert that Acocella et al. teach away from their structure.

The Examiner continues:

Acocella et al. further differ from the claimed invention by not showing a self-aligned source line. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a self-aligned source line because it is a conventional structure in an array of EEPROM devices.

In regards to claim 34, Acocella et al. further disclose the first conductive layer [14] is polysilicon. Acocella et al. differ from the claimed invention by not showing the first " conductive layer having a thickness between about 100 to 500 angstroms It would have been obvious for the first conductive layer having a thickness between about 100 to 500 angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 35, Acocella et al. further disclose the second conductive layer [16] is polysilicon. Acocella et al. differ from the claimed invention by not showing the second conductive layer having a thickness between about 1000 to 3000 angstroms It would have been obvious for the second conductive layer having a thickness between about 1000 to 3000 angstroms, since it has been held that where the general conditions . of a claim are disclosed in the prior art,

discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

The Applicants reply saying that Claims 33, 34 and 35 are dependent on independent claim 29.

Action Item 7

Response to Arguments

As this topic is moot, the Applicants make no response.

Cited Prior Art

We have again reviewed the related art references made of record and agree with the Examiner that none of these suggest the present claimed invention.

CONCLUSION

In light of the above arguments, it is suggested that the Claims clearly distinguish the invention from the prior art. All claims are therefore believed to be in condition for allowance.

Allowance of all claims is therefore respectfully requested.

It is requested that should Examiner Loke not find that the Claims are now Allowable that the Examiner call the undersigned attorney at 914-452-5863, to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B Ackerman, Reg. No. 37,761